Impact of contact resistance on the electrical properties of MoS$_2$ transistors at practical operating temperatures

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Abstract

Molybdenum disulphide (MoS$_2$) is currently regarded as a promising material for the next generation of electronic and optoelectronic devices. However, several issues need to be addressed to fully exploit its potential for field effect transistor (FET) applications. In this context, the contact resistance, R_C, associated with the Schottky barrier between source/drain metals and MoS$_2$ currently represents one of the main limiting factors for suitable device performance. Furthermore, to gain a deeper understanding of MoS$_2$ FETs under practical operating conditions, it is necessary to investigate the temperature dependence of the main electrical parameters, such as the field effect mobility (μ) and the threshold voltage (V_{th}). This paper reports a detailed electrical characterization of back-gated multilayer MoS$_2$ transistors with Ni source/drain contacts at temperatures from $T = 298$ to 373 K, i.e., the expected range for transistor operation in circuits/systems, considering heating effects due to inefficient power dissipation. From the analysis of the transfer characteristics (I_D–V_G) in the subthreshold regime, the Schottky barrier height ($\Phi_B \approx 0.18$ eV) associated with the Ni/MoS$_2$ contact was evaluated. The resulting contact resistance in the on-state (electron accumulation in the channel) was also determined and it was found to increase with T as R_C proportional to $T^{3.1}$. The contribution of R_C to the extraction of μ and V_{th} was evaluated, showing a more than 10% underestimation of μ when the effect of R_C is neglected, whereas the effect on V_{th} is less significant. The temperature dependence of μ and V_{th} was also investigated. A decrease of μ proportional to $1/T^{\alpha}$ with $\alpha = 1.4 \pm 0.3$ was found, indicating scattering by optical phonons as the main limiting mechanism for mobility above room temperature. The value of V_{th} showed a large negative shift (about 6 V) increasing the temperature from 298 to 373 K, which was explained in terms of electron trapping at MoS$_2$/SiO$_2$ interface states.

Introduction

Transition metal dichalcogenides (TMDs) are compound materials formed by the Van der Waals stacking of MX_2 layers (where M = Mo, W, etc., i.e., a transition metal, and X = S, Se, Te, i.e., a chalcogen atom). Among the large number of existing layered materials [1], TMDs are currently attracting increasing scientific interest due to some distinct properties, such as the presence of a sizable bandgap in their band structure. As an example, MoS_2 (the most studied among TMDs due to its high abundance in nature and relatively high stability under ambient conditions) exhibits an indirect bandgap of ≈ 1.3 eV in the case of few layers and bulk material and a direct bandgap of ≈ 1.8 eV in the case of a single layer. These properties make MoS_2 an interesting material for the next generation of electronics and optoelectronics devices [2]. As an example, field effect transistors with very interesting performance in terms of the on/off current ratio (10^6–10^8) and low subthreshold swing (≈ 70 meV/decade) have been demonstrated using single [3] and multilayers of MoS_2 [4].

MoS_2 thin films, obtained either by cleavage from the bulk material or by chemical vapor deposition, are typically unintentionally n-type doped. Since well-assessed methods for doping enrichment of MoS_2 under source/drain contacts are still lacking, MoS_2 transistors are mostly fabricated by deposition of metals directly on the unintentionally doped material, resulting in the formation of Schottky contacts. Experimental investigations showed that both low work function (e.g., Sc, Ti) and high work function (e.g., Ni, Pt) metals mostly exhibit a Fermi level pinning close to the conduction band of MoS_2 [5], resulting in a Schottky barrier height (SBH) for electrons typically ranging from 0.1 to 0.3 eV. The origin of this Fermi level pinning is currently a matter of investigation and a crucial role seems to be played by nanoscale defects/inhomogeneities at the metal/MoS_2 interface [6,7].

The presence of this small but not negligible Schottky barrier at source/drain contacts certainly has a strong impact on the electrical characteristics of MoS_2 transistors in the subthreshold regime [5]. In addition, the resulting source/drain contact resistance, R_C, can also have a significant influence on the electrical properties of the device in the on-state, i.e., above the threshold voltage (V_{th}). In particular, R_C is expected to affect, to some extent, the values of V_{th} and of the field effect mobility μ extracted from the transfer characteristics (drain current, I_D, vs gate bias, V_G) of the device and of the on-resistance (R_{on}) extracted from the output characteristics (drain current, I_D, vs drain bias, V_{DS}). Clearly, all these parameters (V_{th}, μ, and R_{on}) have their own dependence on the temperature, and their combination results in the device electrical characteristics at a fixed measurement condition. Hence, to gain a deeper understanding

of the behavior of MoS_2 transistors for real applications, a temperature-dependent characterization of the main electrical parameters under practical operating conditions is mandatory. A temperature range from room temperature to 400 K is a realistic range for device operation in circuits/systems, taking into account the heating effect they undergo due to inefficient heat dissipation. However, to date, only a limited number of papers have focused on the high temperature behavior of MoS_2 transistors [8,9].

In this paper, we report a detailed temperature dependent investigation of multilayer MoS_2 transistors with Ni source/drain contacts, focusing on the role played by the contact both in the subthreshold regime and above the threshold voltage. In contrast to other literature works, mainly focused on the use of low work function contacts (such as Sc or Ti) to minimize the effect of contact resistance in n-type MoS_2 FETs [5], we focused on a high work function metal such as Ni in this paper in order to evaluate the impact of Ni/MoS_2 contact resistance on the device field effect mobility μ and threshold voltage V_{th}. The interest on Ni was also motivated by the recently demonstrated possibility to achieve MoS_2 FETs with ambipolar behavior by performing a temperature-bias annealing processes on as-deposited Ni contacts [10]. In the following, the temperature dependence of μ, V_{th} and R_C in the range from 298 to 373 K was determined and the physical mechanisms of these dependences were discussed.

Results and Discussion

Back-gated transistors have been fabricated using multilayer MoS_2 flakes (with thickness ranging from ≈ 40 to ≈ 50 nm) exfoliated from bulk molybdenite crystals onto a highly doped Si substrate covered with 380 nm thick, thermally grown SiO_2. Such relatively thick MoS_2 samples have been chosen since it has been reported that the electrical properties (μ, V_{th}) of simple back-gated transistors fabricated with multilayer MoS_2 are much less affected by the effect of the external environment (water/oxygen) [9] with respect to single or few layer devices [11], for which encapsulation is instead required to achieve good electrical performance [3].

Furthermore, as reported in the literature, carrier mobility is only slightly dependent on MoS_2 thickness for transistors fabricated on ≈ 20 to ≈ 70 nm thick flakes, whereas stronger variations are observed for thinner flakes, with the largest mobility values obtained for thicknesses ranging from 6 to 12 nm [5].
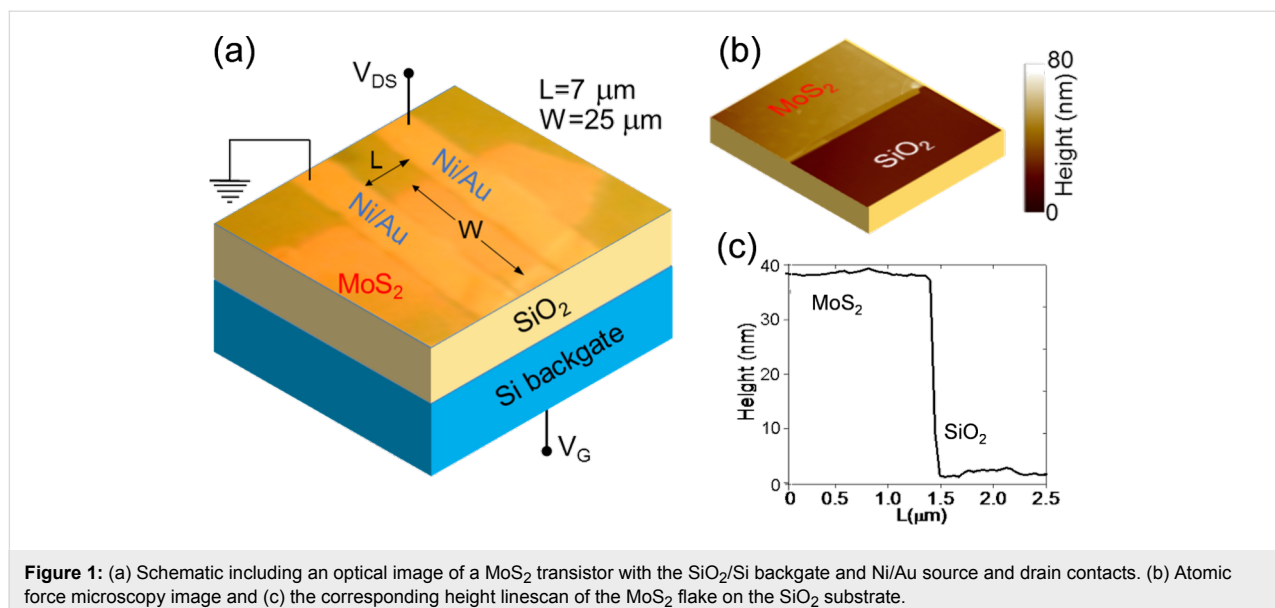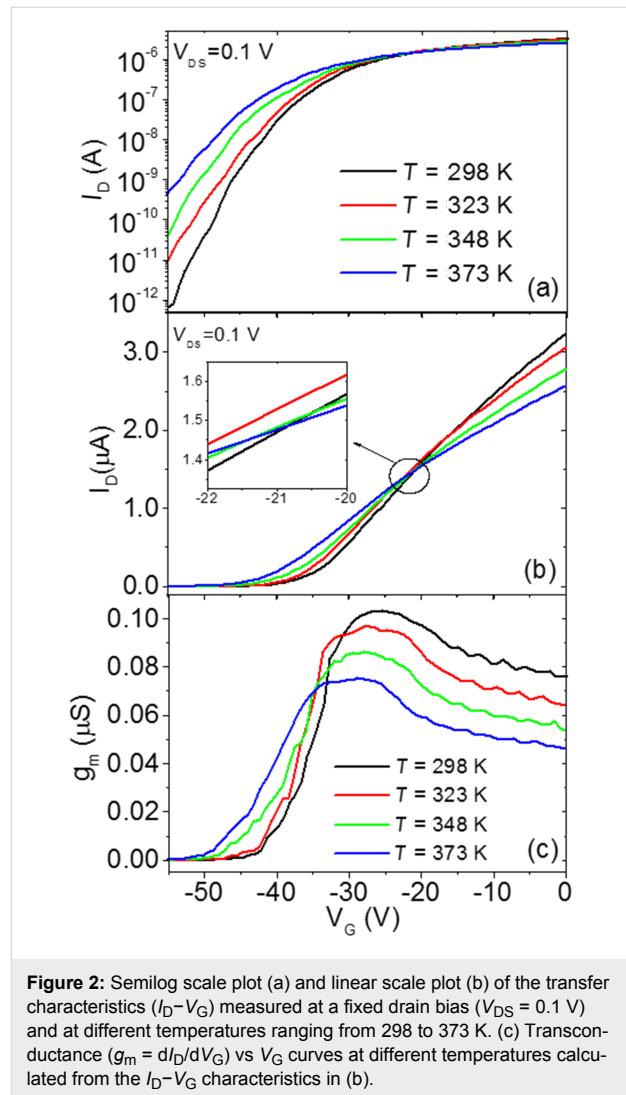
The experiments discussed in this paper have been carried out on a set of ten FETs fabricated on the same substrate. For consistency, the reported temperature-dependent analysis has

been carried out on one of the transistors from this set of devices. Figure 1a shows a schematic representation including an optical image of a MoS_2 transistor with the SiO_2/Si back-gate and Ni/Au source and drain contacts. An atomic force microscopy image (Figure 1b) and the corresponding height linescan (Figure 1c) of the MoS_2 flake on the SiO_2 substrate are also reported, showing ≈40 nm flake thickness.

The transfer characteristics (I_D−V_G) measured at a low fixed drain bias (V_{DS} = 0.1 V) on this device at different temperatures from 298 to 373 K are reported in Figure 2 both on a semilogarithmic scale (Figure 2a) and on a linear scale (Figure 2b). Clearly, the linear scale plot allows the current transport above the threshold voltage (V_{th}) to be studied, whereas the semilog scale plot allows for a better visualization of transport in the subthreshold regime. In the following two sections, a detailed analysis of the characteristics in the subthreshold and above-threshold regime will be reported and the device electrical parameters will be extracted. In particular, the Ni/MoS_2 Schottky barrier height and the flat band voltage (V_{FB}) will be evaluated from the temperature-dependent analysis of the subthreshold I_D−V_G curves, whereas the temperature behavior of V_{th} and μ will be obtained from the curves above the threshold.

Subthreshold behavior

The semilog scale I_D−V_G characteristics (Figure 2a) measured at 298 K exhibit a current variation of more than six orders of magnitude in the bias range from V_G = −55 V to 0 V. This current variation is significantly reduced with increasing the temperature from 298 to 373 K, especially due to the strong increase of current with the temperature at large negative bias.

Figure 2: Semilog scale plot (a) and linear scale plot (b) of the transfer characteristics (I_D−V_G) measured at a fixed drain bias (V_{DS} = 0.1 V) and at different temperatures ranging from 298 to 373 K. (c) Transconductance (g_m = dI_D/dV_G) vs V_G curves at different temperatures calculated from the I_D−V_G characteristics in (b).

Figure 1: (a) Schematic including an optical image of a MoS_2 transistor with the SiO_2/Si backgate and Ni/Au source and drain contacts. (b) Atomic force microscopy image and (c) the corresponding height linescan of the MoS_2 flake on the SiO_2 substrate.

This is better highlighted in Figure 3a, where the I_D–V_G characteristics in the gate bias range from −55 to −35 V and at different temperatures from 298 to 373 K have been reported. Such strong dependence of I_D on T suggests that current transport in the subthreshold regime is dominated by thermionic current injection through the reverse biased source/MoS$_2$ Schottky contact, according to the relation $I_D \propto T^2 \exp\left[-q\Phi_B(V_G)/k_B T\right]$ [5], where $\Phi_B(V_G)$ is the effective Schottky barrier height (SBH), modulated by the gate bias V_G. To verify this, for each V_G an Arrhenius plot of I_D/T^2 vs $1000/T$ is reported in Figure 3b. A nice linear dependence was observed for all the V_G in the considered bias range. The effective SBH values Φ_B, obtained from the slope of the linear fit of the Arrhenius plot in Figure 3b are reported in Figure 3c as a function of V_G. The schematic band diagrams corresponding to the different transistor operation regimes, i.e., depletion (i), flat band (ii) and accumulation (iii), are also illustrated in the inserts of Figure 3c.

In the depletion regime (Figure 3c (i)), the applied gate bias induces an upward band bending, ψ, in MoS$_2$ at the interface with the SiO$_2$ gate insulator. The experimentally evaluated SBH is found to depend linearly on V_G. This dependence can be fitted with the relation $\Phi_B = \Phi_B(V_{FB}) - \gamma(V_G - V_{FB})$, where

$\Phi_B(V_{FB})$ is the effective SBH at the flat band voltage and the term $\psi = \gamma(V_G - V_{FB})$ is the upward band bending. The slope γ indicates the modulation efficiency of Φ_B by the gate bias. It depends on the SiO$_2$ layer capacitance, $C_{ox} = \varepsilon_0\varepsilon_{ox}/t_{ox} \approx 9.1 \times 10^{-5}$ F/m^2 (ε_0 is the vacuum dielectric constant, $\varepsilon_{ox} = 3.9$, $t_{ox} = 380$ nm, the permittivity and the thickness of the SiO$_2$ film, respectively), on the capacitance of the MoS$_2$ depletion region, C_s, as well as on the capacitance associated with MoS$_2$/SiO$_2$ interface traps, C_{it} [5]. In the depletion regime, the current transport in the transistor is ruled by thermionic emission (TE) of electrons from the source contact to the channel.

The effective SBH Φ_B and, hence, the band bending $\psi = \Phi_B(V_G) - \Phi_B(V_{FB})$ is found to decrease linearly moving toward positive V_G values. The flat band voltage V_{FB} corresponds to the gate bias for which $\psi = 0$ (see (ii) in Figure 3b), whereas for $V_G > V_{FB}$ the band bending $\psi < 0$ (see (iii) in Figure 3b), i.e., the channel starts to accumulate electrons. In the accumulation regime, current injection in the channel is ruled by thermionic field emission (TFE) through the source triangular barrier. The TFE mechanism yields a reduced effective SBH with respect to the constant Φ_B value (red dashed line in Figure 3c) that would be expected if only TE over the barrier would occur. As a guide
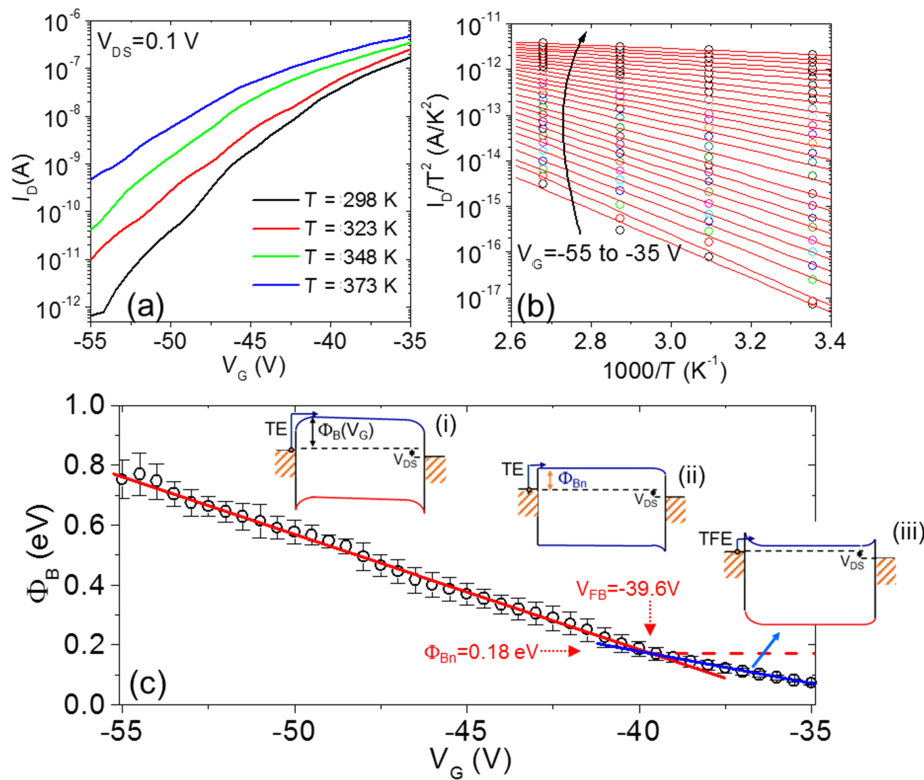

Figure 3: (a) Semilog scale plot of the transfer characteristics (I_D–V_G) in the subthreshold regime at different temperatures ranging from 298 to 373 K. (b) Arrhenius plot of I_D/T^2 vs $1000/T$ for each gate bias. (c) Effective SBH Φ_B as a function of V_G. In the inserts, schematic band diagrams are given for the transistor operation in different regimes: depletion (i), flat band voltage (ii) and accumulation (iii).

for the eye, the SBH dependence on V_G in the accumulation regime has been fitted with a blue line in Figure 3c. Hence, $V_{FB} = -39.6$ V can be experimentally determined as the bias corresponding to the intercept between the two linear fits [5]. The corresponding SBH value $\Phi_B(V_{FB}) = 0.18$ eV represents the "real" (i.e., gate bias independent) value of the Ni/MoS$_2$ Schottky barrier.

The experimental V_{FB} for the MoS$_2$ transistor exhibits a large negative value, as reported in other literature works [12]. Such a result has been ascribed to donor-like interface trap states (positively charged when empty) between the SiO$_2$ and MoS$_2$ [13,14]. In order to evaluate the amount of this positive charge at the interface, it is worth comparing the experimental value with the one deduced from theoretical expression of the flat band voltage ($V_{FB,id}$) of an ideal metal-oxide-semiconductor field effect transistor (i.e., without fixed or interface charges). $V_{FB,id}$ is expressed as [15]:

$$V_{FB,id} = W_M - \left[\chi + E_G/2 - kT/q \ln\left(N_D/n_i\right) \right], \quad (1)$$

where W_M is the work function of the gate material (4.05 eV for the n$^+$-doped Si back gate in our transistor), χ is the semiconductor electron affinity (4.2 eV for MoS$_2$), N_D is the semiconductor doping concentration (on the order of 10^{16} cm^{-3} in unintentionally doped MoS$_2$) and n_i is the intrinsic carrier concentration (for MoS$_2$, $n_i \approx 6\times10^{15}T^{3/2}\exp\left(-E_G/2kT\right)$ cm^{-3}). According to this expression a low value of $V_{FB,id}$ slightly varying with the T (from -0.35 V at 298 K to -0.42 V at 273 K) would be expected for our device. The negative shift of the experimental V_{FB} with respect to $V_{FB,id}$ can be accounted for by the presence of a net positive charge density at the interface with SiO$_2$ that can be evaluated as $C_{ox}(V_{FB}-V_{FB,id})/q \approx 2.2 \times 10^{12}$ cm^{-2}.

In the following section, the device transfer characteristics above the threshold will be analyzed to extract the threshold voltage and mobility.

Transfer characteristics above threshold

The linear scale transfer characteristics (Figure 2b) show very low current below a threshold voltage (V_{th}) and a nearly linear increase of I_D vs V_G above V_{th}. Two effects can be observed from the comparison of the I_D-V_G curves at increasing temperatures, i.e., (i) a negative shift of the threshold voltage and (ii) a decrease of the I_D-V_G curve slope in the linear region above V_{th}. The origin of these two effects will be discussed more in detail later on. Interestingly, as a result of these two competing effects, the I_D-V_G characteristics tend to cross nearly at the same gate bias $V_G = -21$ V (see details in the insert of Figure 2b). This bias condition can be interesting for some ap-

plications where it is desirable that the device performance does not depend significantly on the temperature (dI_D/d$T \approx 0$).

Figure 2c shows the transconductance g_m vs V_G curves calculated by differentiation ($g_m = dI_D/dV_G$) of the I_D-V_G characteristics in Figure 2b. In the considered bias range, all the curves exhibit an increase of g_m with V_G up to a maximum value, followed by a decrease of g_m. The maximum transconductance value ($g_{m,max}$) is found to decrease with increasing temperature. Furthermore, a rigid shift of the g_m-V_G curves toward negative gate bias values is observed with increasing T.

From the linear scale transfer characteristics and the transconductance, two key electrical parameters for transistor operation, i.e., the threshold voltage (V_{th}) and the field effect mobility (μ), are typically evaluated. Figure 4a shows a linear scale plot of I_D (left axis) and of the transconductance g_m (right axis) at $V_{DS} = 0.1$ V and $T = 298$ K. The field effect mobility in the linear region, μ_{lin}, of the transfer characteristics is typically extracted from the transconductance using the following formula $\mu_{lin} = g_m L/(W C_{ox} V_{DS})$, where L and W are the channel length and width, respectively, and C_{ox} the SiO$_2$ gate capacitance. For our device with $L/W = 7$ μm/25 μm and $C_{ox} \approx 9.1 \times 10^{-5}$ F/m^2, the evaluated mobility from the maximum transconductance value $g_{m,max}$ was $\mu_{lin} = 31.75$ cm^{2}V^{-1}s^{-1}, as indicated in Figure 4a. A method for evaluating V_{th} consists of drawing the tangent line to the I_D-V_G curve at the bias ($V_{G,max}$) corresponding to $g_{m,max}$ and taking the intercept with the $I_D = 0$ baseline [16], as shown in Figure 4a.
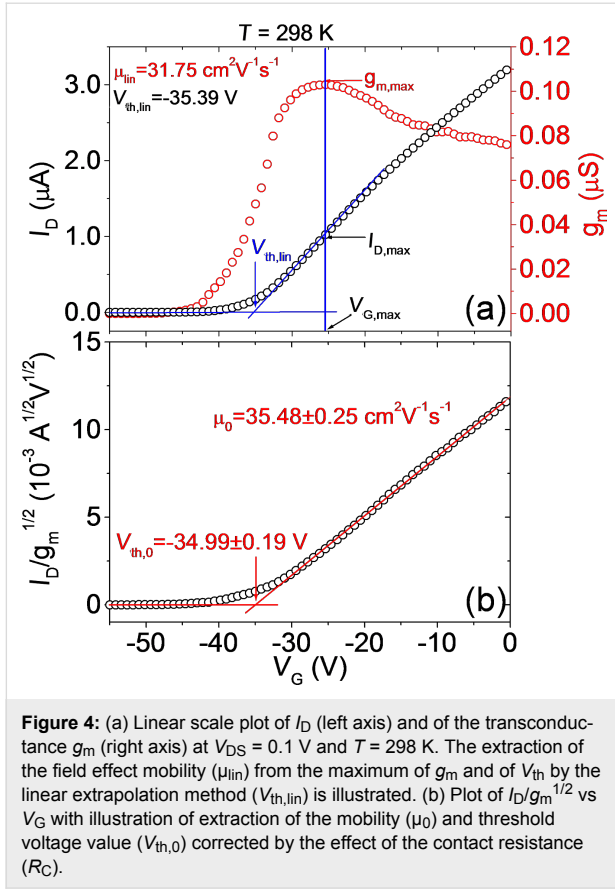
This procedure can be explained by simple geometrical considerations. In the linear region of the transfer characteristics, I_D can be expressed as [14]:

$$I_D = \frac{W}{L}\mu C_{ox}V_{DS}\left(V_G - V_{th}\right). \quad (2)$$

Hence, it results that $I_{D,max} = g_{m,max}(V_{G,max}-V_{th})$ and the threshold voltage can be calculated as

$$V_{th,lin} = -I_{D,max}/g_{m,max} + V_{G,max} \approx -35.39\,\text{V}.$$

As a matter of fact, for the evaluation of $V_{th,lin}$ and μ_{lin} based on Equation 2 the contribution of the contact resistance is assumed to be zero. However, as deduced from the analysis of the subthreshold characteristics, a Schottky barrier is associated to the source/drain contacts with MoS$_2$, which is also expected to result in a non-negligible contact resistance, R_C. The value of the contact resistance above the threshold and its temperature dependence will be estimated in the last section of this paper from the analysis of the on-resistance (R_{on}) extracted from the

Figure 4: (a) Linear scale plot of I_D (left axis) and of the transconductance g_m (right axis) at $V_{DS} = 0.1$ V and $T = 298$ K. The extraction of the field effect mobility (μ_{lin}) from the maximum of g_m and of V_{th} by the linear extrapolation method ($V_{th,lin}$) is illustrated. (b) Plot of $I_D/g_m^{1/2}$ vs V_G with illustration of extraction of the mobility (μ_0) and threshold voltage value ($V_{th,0}$) corrected by the effect of the contact resistance (R_C).

device output characteristics (I_D–V_{DS}) at low V_{DS}. Here, we want to discuss how R_C can influence the evaluation of μ and V_{th} from the transfer characteristics.

In order to take into account the role of R_C, V_{DS} can be replaced by $V_{DS} - I_D R_C$ in Equation 2, and solving by I_D, the following expression for I_D is obtained:

$$I_D = \frac{\frac{W}{L} \mu_0 C_{ox} V_{DS} \left(V_G - V_{th,0} \right)}{1 + \frac{W}{L} \mu_0 C_{ox} R_c \left(V_G - V_{th,0} \right)}, \qquad (3)$$

where μ_0 and $V_{th,0}$ represent the values of the mobility and threshold voltage corrected by the effect of R_C. As a consequence, the transconductance $g_m = dI_D/dV_G$ can be expressed as:

$$g_m = \frac{\frac{W}{L} \mu_0 C_{ox} V_{DS}}{\left[1 + \frac{W}{L} \mu_0 C_{ox} R_c \left(V_G - V_{th,0} \right) \right]^2}. \qquad (4)$$

Noteworthy, the ratio $I_D / \sqrt{g_m} = \sqrt{W/L \, \mu_0 C_{ox} V_{DS}} \left(V_G - V_{th,0} \right)$ is independent of R_C. A plot of $I_D/g_m^{1/2}$ vs V_G is reported in Figure 4b. The corrected value of the field effect mobility ($\mu_0 = 35.48 \pm 0.25$ cm^{2}V^{-1}s^{-1}) can be calculated from the slope of the linear fit of these data, whereas the threshold voltage ($V_{th,0} = -34.99 \pm 0.19$ V) can be obtained from the intercept with the x axis. It is worth noting that the mobility value μ_0 after correction for the contact resistance is more than 10% higher than the value estimated without any correction, whereas the threshold voltage $V_{th,0}$ after correction is only 1% higher than the value estimated without accounting for R_C. This indicates that the underestimation of the mobility neglecting the contact resistance effect can be quite relevant, whereas the threshold voltage is less affected by R_C. By repeating this procedure for all the measured characteristics reported in Figure 2b,c, the temperature dependence of the mobility (μ_{lin} and μ_0), threshold voltage (V_{th} and $V_{th,0}$) in the considered temperature range has been evaluated, as illustrated in Figure 5a,b, respectively.

Both μ_{lin} and μ_0 were found to decrease as a function of T with a similar dependence $1/T^\alpha$, with $\alpha = 1.5 \pm 0.2$ in the case of μ_{lin} and $\alpha = 1.4 \pm 0.3$ in the case of μ_0. Such a dependence of $\mu \approx 1/T^\alpha$ with $\alpha > 1$ indicates that the main mechanism limiting the mobility of electrons in the multilayer MoS$_2$ channel in this temperature range is scattering by optical phonons, as reported by other experimental and theoretical investigations [4]. Instead, electron mobility was found to be limited by Coulomb scattering by charged impurities only at lower temperatures (<100 K) [4]. Noteworthy, scattering by charged impurities at the interface with the substrate results in the dominant mechanism for another well-studied 2D material, graphene, even at room temperature and higher temperatures [17,18].

In Figure 5b, the threshold voltage V_{th} exhibits a negative shift of about 6 V with increasing the temperature from 298 to 273 K. For convenience, the difference $V_{th} - V_{FB}$ is also reported in Figure 5b, right scale. It is useful to compare the experimental temperature dependence of V_{th} with the expected theoretical variation with temperature, in order to understand which are the relevant physical parameters ruling this behavior.

For an ideal transistor (without interface states) operating under accumulation conditions, the shift between the threshold voltage $V_{th,id}$ and the flat band voltage $V_{FB,id}$ can be expressed as:

$$V_{th,id} - V_{FB,id} = \psi_{th} + \frac{q N_s \left(\psi_{th} \right)}{C_{ox}} \qquad (5)$$

where ψ_{th} is the downward (negative) band bending at the threshold (as illustrated in the band diagram (iii) of Figure 3c,
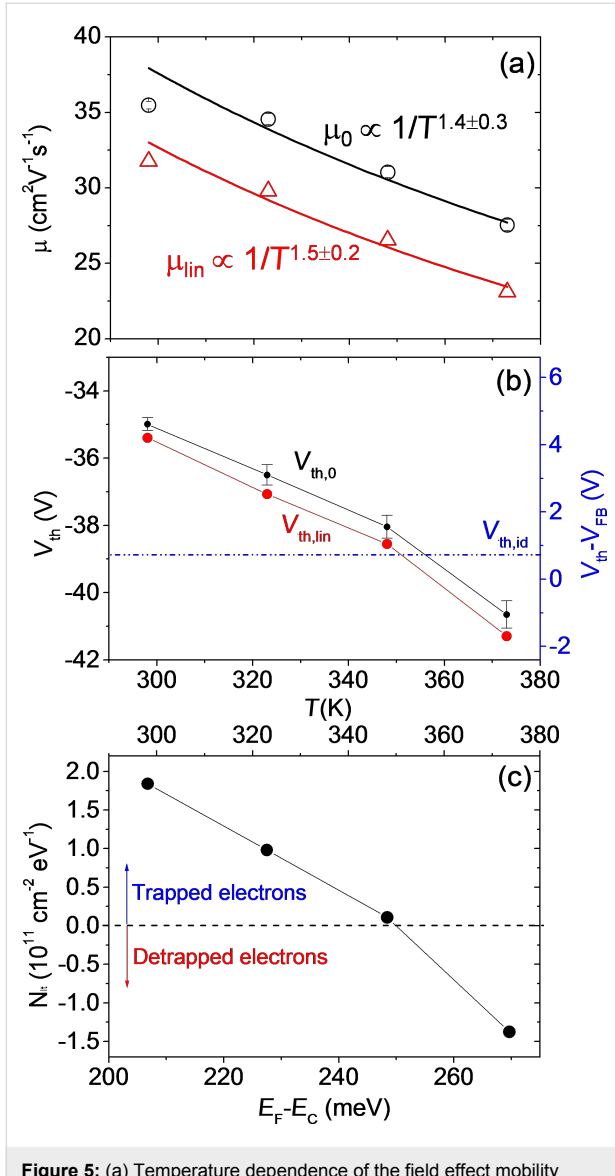
Figure 5: (a) Temperature dependence of the field effect mobility extracted from the linear region of the I_D−V_G characteristics without (μ_{lin}) and with (μ_0) the correction for the effect of the contact resistance R_C. Experimental data have been fitted with a temperature dependence $1/T^\alpha$. (b) Temperature dependence of the threshold voltage evaluated without ($V_{th,lin}$) and with ($V_{th,0}$) the correction for the effect of the contact resistance R_C. (c) Density of trapped/detrapped electrons at MoS$_2$/SiO$_2$, as a function of T (upper scale) and the corresponding position of the Fermi level with respect to the conduction band (E_F−E_C).

and $N_s(\psi_{th})$ is the electron density in the channel at ψ_{th}

$$N_s\left(\psi_{th}\right) = \frac{\sqrt{2}\varepsilon_0\varepsilon_s}{kTL_D}\sqrt{\left[\exp\left(-\frac{\psi_{th}}{kT}\right) + \frac{\psi_{th}}{kT} - 1\right]}, \quad (6)$$

where $L_D = \sqrt{\varepsilon_0\varepsilon_s kT/q^2 N_D}$ is the Debye length. The band bending ψ_{th} can be evaluated assuming that the electron density in the channel at the threshold corresponds to $N_s(\psi_{th}) = tN_D$,

where N_D is the uniform doping concentration in the MoS$_2$ thin film and t its thickness. Assuming $N_D = 10^{16}$ cm^{-3} for our unintentionally doped MoS$_2$, we obtain $N_s \approx 4 \times 10^{10}$ cm^{-2}. Furthermore, a value of ψ_{th} ranging from approximately −34 meV (at $T = 298$ K) to −39 meV (at $T = 373$ K) can be estimated from the dependence of N_s on ψ_{th} in Equation 6. Under these assumptions, $V_{th,id}−V_{FB,id} \approx 0.7$ eV (nearly independent of T) can be estimated, as indicated in Figure 5b (blue dashed line).

In order to account for the large change of V_{th} with temperature, the role of interface states at SiO$_2$/MoS$_2$ interface must be considered. The difference between the experimental $V_{th}−V_{FB}$ and theoretical $V_{th,id}−V_{FB,id}$ can be described by a term $\Delta V_{it} = qN_{it}/C_{ox}$, where N_{it} is the density of trapped/detrapped electrons by SiO$_2$ interface traps. These interface traps exhibit a donor like behavior, i.e., they are positively charged above the Fermi level (when they are empty) and neutral below the Fermi level (when they are filled by electrons) [13]. Hence, electron trapping results in a neutralization of the interface states, resulting in a positive shift of V_{th} with respect to V_{FB} (i.e. $\Delta V_{it} > 0$). On the contrary, detrapping of electrons from these states results in an increase of the positive charge and, hence, in $\Delta V_{it} < 0$.

From the experimental data in Figure 5b, trapped electron densities $N_{it} = 2 \times 10^{11}$, 1×10^{11}, and 2×10^{10} cm^{-2} are estimated at 298, 323, and 348 K, respectively, whereas a detrapped electron density $N_{it} = 1.3 \times 10^{11}$ cm^{-2} is obtained at 373 K (see Figure 5c). Electron trapping and detrapping at MoS$_2$/SiO$_2$ interface have been shown to be thermally activated processes [13]. Hence, for a given interface trap distribution D_{it} close to the MoS$_2$ conduction band, N_{it} can be expressed as

$$N_{it} = \left[P_{tr}(T) - P_{det}(T)\right]\int_{E_F-E_C+\psi}^{E_F-E_C} D_{it}\,d\phi \quad (7)$$

where $P_{tr}(T)$ and $P_{det}(T)$ are the trapping and detrapping probabilities, respectively [13]. The experimentally found temperature dependence of N_{it} can be explained as follows. As T increases, the shift of the Fermi energy E_F with respect to E_C increases as

$$E_F - E_C = \frac{E_G}{2} - \frac{kT}{q}\ln\left[\frac{N_D}{n_i(T)}\right]$$

resulting in a change of the integration range in Equation 7. Furthermore, the difference $P_{tr}(T)−P_{det}(T)$ can change with T. The dependence of N_{it} on E_F is also illustrated in Figure 5c. It is consistent with a decrease of D_{it} with increasing E_F−E_C.

Furthermore, at 373 K, it can be argued that the P_{det} becomes higher than P_{tr}, resulting in a negative value of N_{it}.

Output characteristics

Figure 6 shows the output characteristics I_D−V_{DS} for different gate bias values ranging from $V_G = -56$ to 0 V (with steps $\Delta V = 4$ V) measured at different temperatures, i.e., (a) 298 K, (b) 323 K, (c) 348 K and (d) 373 K. For all the V_G values, I_D exhibits a linear increase with V_{DS} at low drain bias ($V_{DS} \ll V_G - V_{th}$), whereas it deviates from the linear behavior at larger V_{DS}. In particular, current saturation is achieved whenever the condition $V_{DS} > V_G - V_{th}$ is reached. By comparing the output characteristics measured at the different temperatures with the same V_G values, it is evident that both the slope of the I_D−V_{DS} curves in the linear region and the saturation current value decreases with increasing T.

The reciprocal of the I_D−V_{DS} curves slope in the linear region at low V_{DS} is the device on-resistance R_{on}, which can be expressed as:

$$R_{on} = 2R_C + \frac{L}{W}R_{ch} = 2R_C + \frac{L}{W}\frac{1}{q\mu(V_G - V_{th})}, \qquad (8)$$

where R_C is the source and drain contact resistance and R_{ch} the channel sheet resistance, which depends inversely on ($V_G - V_{th}$), according to Equation 2.

Figure 7a reports the plots of R_{on} vs $1/(V_G - V_{th,lin})$ extracted from the I_D−V_{DS} characteristics in Figure 6 at the different temperatures. The linear fit of the data was performed for the four temperatures and, from the intercept with the vertical axis, the value of the contact resistance R_C was estimated. The behavior of R_C vs T is reported in Figure 7b, indicating an increase of $R_C \propto T^{\alpha}$, with $\alpha = 3.1 \pm 0.3$.

Finally, the behavior of the output characteristics at high V_{DS} is discussed. Figure 8a shows the I_D−V_{DS} characteristics measured at $T = 298$ K. The $V_G - V_{th}$ value for each curve is indicated. It can be observed that the current saturation regime (i.e., I_{DS} in-
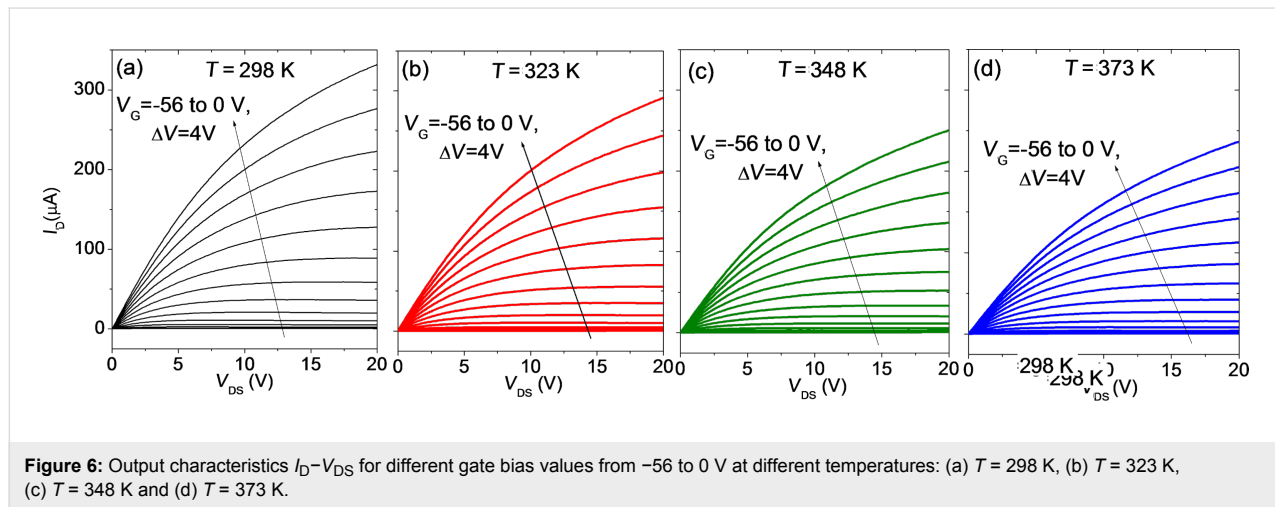

Figure 6: Output characteristics I_D−V_{DS} for different gate bias values from −56 to 0 V at different temperatures: (a) $T = 298$ K, (b) $T = 323$ K, (c) $T = 348$ K and (d) $T = 373$ K.
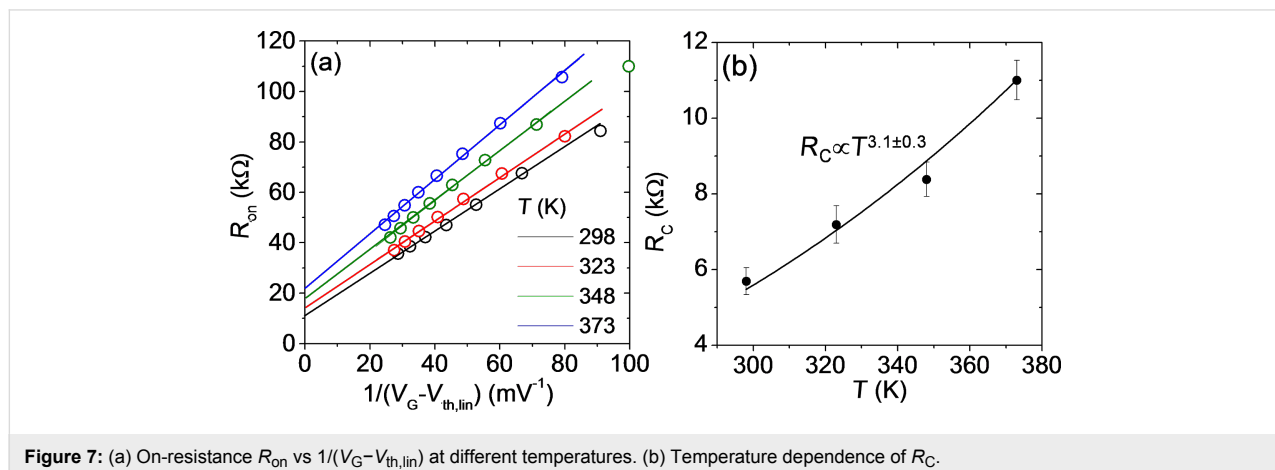

Figure 7: (a) On-resistance R_{on} vs $1/(V_G - V_{th,lin})$ at different temperatures. (b) Temperature dependence of R_C.
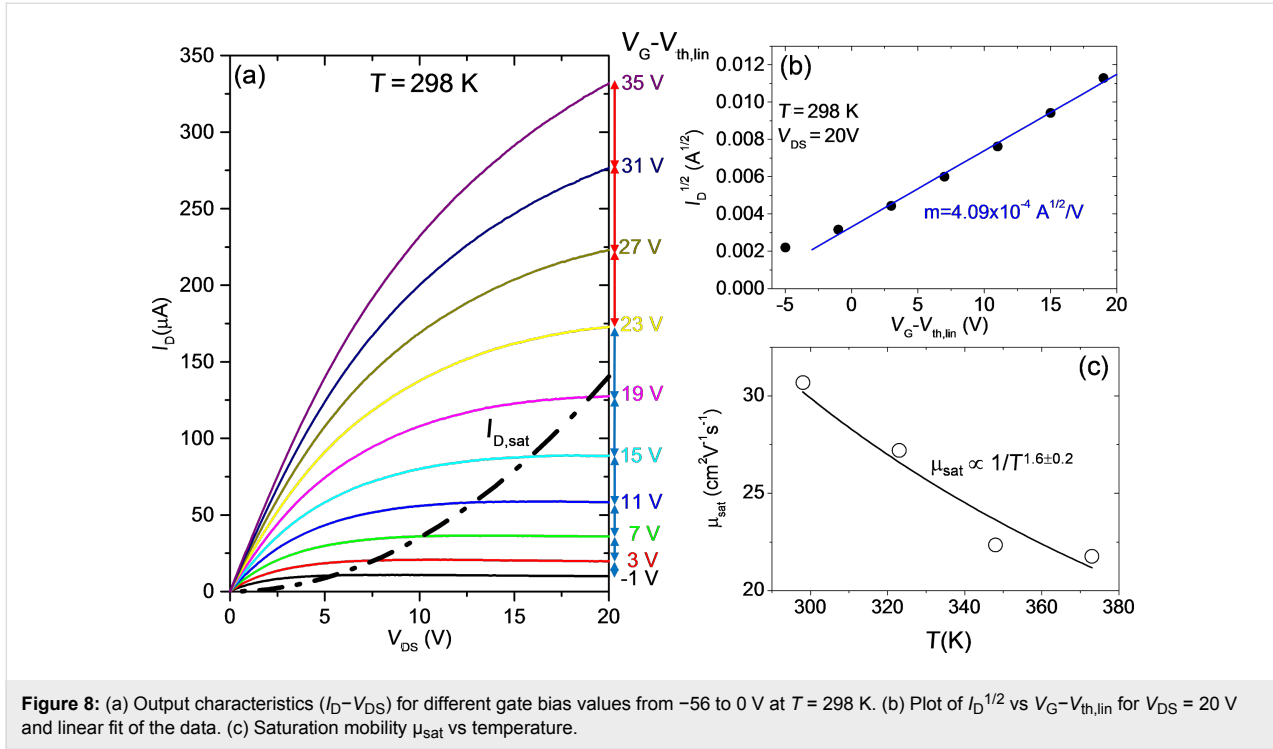
Figure 8: (a) Output characteristics (I_D−V_{DS}) for different gate bias values from −56 to 0 V at *T* = 298 K. (b) Plot of $I_D^{1/2}$ vs V_G−$V_{th,lin}$ for V_{DS} = 20 V and linear fit of the data. (c) Saturation mobility μ_{sat} vs temperature.

dependent of V_{DS}) is reached only for V_G−V_{th} < 20 V, corresponding to an accumulated electron density in the channel N_s < 1.1 × 10^{12} cm^{-2}. For V_G−V_{th} > 20 V, saturation is not reached.

In the saturation condition, I_D is only a quadratic function of V_G−V_{th} [14]:

$$I_{D,sat} = \frac{W}{2BL}\mu_{sat}C_{ox}\left(V_G - V_{th}\right)^2,\qquad(9)$$

where μ_{sat} is the mobility value under saturation conditions and the term *B* is the so-called body coefficient, which depends on the gate oxide capacitance, on the doping concentration in the film and on the temperature:

$$B = 1 + \frac{1}{2C_{ox}}\sqrt{\frac{\varepsilon_0\varepsilon_s q^2 N_D}{kT\ln\left[N_D/n_i\left(T\right)\right]}}.$$

For thin gate dielectrics and low doping in the film, *B* can be approximated to 1, but for thick dielectrics and high doping its value can be significantly higher. In the case of our device with C_{ox} = 9.1 × 10^{-5} F/m and assuming a MoS$_2$ doping N_D ≈ 1 × 10^{16} cm^{-3}, *B* can range from ≈2.97 to ≈3.12 in the considered temperature range. In Figure 8b, $I_D^{1/2}$ at V_{DS} = 20 V is reported as a function of V_G−V_{th}, showing a linear behavior. According to Equation 9, the mobility under saturation condi-

tion can be evaluated from the slope *m* of the fit, as $\mu_{sat} = 2BLm^2/WC_{ox}$. By repeating this procedure for all the output characteristics measured at the different temperatures, the behavior of μ_{sat} as a function of *T* can be obtained. The main error source in the estimation of μ_{sat} is related to the fact that the doping concentration N_D and, hence, the coefficient *B* is not exactly known. Noteworthy, the values of μ_{sat} in Figure 8c, estimated assuming N_D ≈ 1 × 10^{16} cm^{-3}, are very close to those evaluated from the linear region of the transfer characteristics (see Figure 5a) and exhibit a similar temperature dependence. This also confirms that the assumption for the doping concentration is correct.

Conclusion

In conclusion, a temperature dependent investigation of back-gated multilayer MoS$_2$ transistors with Ni source/drain contacts in the range from *T* = 298 to 373 K has been performed. The SBH Φ_B ≈ 0.18 eV of the Ni/MoS$_2$ contact was evaluated from the analysis of the transfer characteristics I_D−V_G in the subthreshold regime. The resulting R_C associated with the SBH was determined by fitting the R_{on} dependence on $1/(V_G$−$V_{th})$ extracted from the device output characteristics I_D−V_{DS} at low V_{DS}. An increase of $R_C \propto T^{3.1}$ was demonstrated. The impact of R_C on the values of μ and V_{th} values was determined, showing an underestimation of μ by more than 10% if the effect of R_C is neglected, whereas the influence of R_C on the estimated value of V_{th} is only 1%. Furthermore, the temperature dependence of μ and V_{th} was investigated, showing a decrease of

$\mu \approx 1/T^{\alpha}$ with $\alpha = 1.4 \pm 0.3$ (indicating scattering by optical phonons as the limiting mechanism), and a negative shift of V_{th} by about 6 V with increasing T. The role played by electron trapping at the MoS_2/SiO_2 interface to explain such a large V_{th} shift was discussed.

Experimental

Back-gated transistors were fabricated using MoS_2 flakes exfoliated from molybdenite bulk crystals (supplier SPI [19]) with thicknesses ranging from ≈40 to ≈50 nm and transferred onto a highly doped n-type Si substrate covered with 380 nm of thermally grown SiO_2. An accurate sample preparation protocol has been adopted for controlled quality of the MoS_2/SiO_2 interface, as this is crucial to achieve reproducible electrical behavior of the devices. In particular, thermo-compression printing using a Karl-Suss nanoimprint device with fixed temperature and pressure conditions [20,21] has been employed to transfer the exfoliated MoS_2 flakes onto the SiO_2 surface that was previously cleaned using solvents and a soft O_2 plasma treatment. Finally, source and drain contacts were obtained by deposition and lift-off of a Ni(50 nm)/Au(100 nm) bilayer.

The temperature-dependent electrical characterization in the range from 298 to 373 K was performed using a Cascade Microtech probe station with an Agilent 4156b parameter analyzer. All the measurements were carried out in dark conditions and under nitrogen flux.

Acknowledgements

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